trench, to the third covering layer and to the substrate, respectively;

wherein the difference d_1-d_2 of said first and second depths d_1 and d_2 is sufficient to force junction breakdown away from the trench and into the heavily doped portion of the second covering layer.

54. (Amended) A semiconductor device comprising:

a semiconductor [body] substrate having a trench therein of depth d_{tr} and substantially vertical side walls, said semiconductor substrate including a drain region, a source region, a body region, and a gate region within said trench and separated from said body region by a dielectric material, said body region having a maximum depth of d_{max}, wherein said maximum depth d_{max} being greater than said depth d_{tr} by an amount sufficiently large to force junction breakdown away from said trench.

~~56~~ 37. (Amended) A semiconductor device as in claim ~~55~~ 34 wherein the epitaxial layer has a top surface and the body region extends from ~~the top~~ surface of the epitaxial layer [top surface] into an upper portion of the epitaxial layer.

~~58~~ 39. (Amended) A semiconductor device as in Claim ~~54~~ 35 wherein said body region extends upward through the epitaxial layer [region] and forming an exposed pattern at ~~the top~~ surface of said epitaxial layer [top surface].

REMARKS

Claims 17-42 and 44-66 were pending prior to this Amendment. Claims 45 and 66 are cancelled. Claims 30, 42, 54, 56, 58, 63 and 64 are amended.

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The Examiner objected to the figures, stating:

> Under 37 C.F.R. 1.83(a) we newly object to the Figures because they do not show every feature of the subject matter required by newly presented Claims 63 and 66. Claim 63, like Claim 42, more particularly requires a
>
> > "second polysilicon layer extends from the trench to a field region creating an electrical contact to the metal layer",
>
> excerpted from the last four Claim lines. Figure 31B instead shows a first polysilicon layer (36) extending from a trench in the active region to a termination region where it electrically contacts metal (43a). No Figure shows the a second polysilicon layer extension as required by Claim 63. Claim 66, like Claim 45, more particularly requires a horizontal cross section of a semiconductor body to have a substantially "circular shape" . No figure shows a semiconductor body having a circular shape. In response we therefore require either a showing in the Figures of the subject matter required by each of Claims 63 and 66, as excerpted supra, but without the introduction and further introduction of new matter prohibited under at least 35 U.S.C. 132, or we require deletion of the excerpts supra from the claimed subject matter.

Claims 42 and 63 are each amended to recite "a metal layer wherein said first polysilicon layer extends from the trench to a field region creating an electrical contact" which is clearly shown in Figures 31A and 31B. Claims 45 and 66 are now cancelled. Applicants respectfully submit that the Examiner's objection to the figures are no longer warranted.

The Examiner rejected Claim 30-31, 42, 58-59, 63-64 under 35 U.S.C. § 112, second paragraph, as being vague and indefinite, stating:

> More particularly with respect to Claim 30, there is no antecedent basis for
>
> > "the exposed pattern of the second covering layer at the top surface of the third covering layer",
>
> recited on Claim lines 39 through 41. Furthermore Claim lines 56-7 require
>
> > "junction breakdown away from the trench and into the."

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> thus requiring a reader to speculatively discern that into which breakdown occurs. Claim 31 is thereby vague and indefinite due to its dependency upon vague and indefinite Claim 30, discussed supra. Claim 58 is vague and indefinite because there are no antecedent bases for "the epitaxial region", "the epitaxial layer" and "the epitaxial layer top surface". Claim 59 is vague and indefinite thereby due to its dependency upon vague and indefinite Claim 58, discussed supra. Claim 63, like Claim 42, requires subject matter not originally disclosed and not originally possessed by the Applicants at the time the Invention was made. Claims 42 and 63 thereby require new matter expressly prohibited under 35 U.S.C. 132 because the subject matter claimed has no basis whatsoever in the original disclosure. We therefore additionally reject Claims 42 and 63 under the first paragraph of 35 U.S.C. 112 because they require new matter not originally disclosed. Claim 64 is vague and indefinite because there are no antecedent bases for "the gate region", "the drain region" and "the source region."

Claims 30, 42, 56, 58 and 63 are amended to correct the deficiencies pointed out by the Examiner. Claim 64 is amended to depend from Claim 54 which, as amended, provides antecedent bases for the gate region, the drain region and the source region recited in Claim 64. As amended, Applicants believe that Claims 30-31, 58-59 and 63-64 fully comply with 35 U.S.C. § 112.

With respect to Applicants' arguments presented on December 26, 1995 the Examiner states:

> The Applicants indicated on amendment page 9 that at least Claim 17 requires a topological distinction over the V-shaped insulated gate transistor illustrated by Tonnel in Figures 3, 6 through 12 and 14 through 19.
>
> In response, we agree. However, we decline to overlook the fact that Tonnel further expected to alternatively form insulated gate transistors whereby the insulated gate electrode is accommodated within slots having vertical sides, evidently from the paragraph spanning columns 5 and 6. Tonnel found thereby that one would have advantageously increased packing density. Observing that Ueda et al., Reference AR provided by the Applicants on 02 July 1993, similarly found the higher packing density advantage when using insulated gate transistors whereby the insulated gate electrode is accommodated within slots having vertical sides, we thus conclude that Tonnel

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> alternatively expected to accommodate insulated gate electrodes within slots like those shown by Ueda et al. with Figure 1.

Applicants respectfully disagree with the Examiner, Tonnel merely states:

> The procedure described above can also be applied with a substrate orientation (110) instead of (100). In this case, the slots have vertical sides and it is then possible to reduce even more the spacing of the interdigital structure... (Tonnel's col. 5, lines 61-65)

To support his contention that Tonnel teaches Claim 17's limitations, the Examiner relies merely on Tonnel's figures 3, 12 and 19, which are believed not to have been drawn to scale and fortuitously show a V-groove having a depth less than the maximum depth of the body region (See Paper 14, Office Action of June 8, 1994, and subsequent Office Actions). However, Tonnel's Specification does not provide any verbal description with respect to the relative depths of the body region and its V-groove. Thus, Applicants respectfully submit that the above-quoted teaching of Tonnel neither suggests nor discloses the relative depths of the body region and a slot with vertical side walls, the above-quoted teaching of Tonnel providing no teaching regarding the relative depths of this hypothetical vertical trench and the body region. Further, Ueda et al. teach a trench having a depth exceeding the depth of the body region. Thus, without specific teaching regarding the relative depths of the body region and the hypothetical vertical trench, Tonnel's and Ueda et al.'s combined teachings do not disclose or suggest Applicants' Claim 17.

The Examiner rejected Claims 17-22, 24-29, 30, 31, 32-37, 44, 64-65, 46-49, 51-58 under 35 U.S.C. § 103 as being unpatentable over considerations of Tonnel and Ueda et al., as discussed in the previous Office Actions.

Applicants respectfully submit that the Examiner's rejection of Claims 17-22, 24-29, 30, 31, 32-37, 44, 64-65, 46-49, and 51-58 under 35 U.S.C. § 103 is erroneous. For reasons

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already discussed above, without specific teaching regarding the relative depths of the body region and the hypothetical vertical trench, Tonnel's and Ueda et al.'s combined teachings do not disclose or suggest Applicants' Claim 17-22, 24-29, 30, 31, 32-37, 44, 64-65, 46-49, and 51-58.

The Examiner also rejects Claim 50 under 35 U.S.C. § 103 as being unpatentable over considerations of Tonnel, Ueda et al. and Lisiak et al.

Applicants respectfully traverse the Examiner's rejection of Claim 50 under 35 U.S.C. § 103. Since Lisiak et al. teach a V-groove having a depth greater than the depth of the body region exceeding the depth of the body region (Lisiak's Fig. 1), Applicants respectfully submit that the combined teachings of Tonnel, Ueda et al., and Lisiak et al. do not disclose or suggest Claim 50.

The Examiner rejected Claims 39-41 and 60-62 under 35 U.S.C. § 103 as being unpatentable over considerations of Tonnel, Ueda et al. and Yamabe et al., stating:

> Yamabe et al. taught at least the leakage current advantage of performing etching to remove a sacrificial oxide layer to round corners of trenches accommodating insulated gate electrodes, like those anticipated by Ueda et al. and envisaged by Tonnel. We thus conclude it to have been obvious for one to have performed rounding of trenches accommodating insulated gate electrodes to gain the leakage current advantage in trench insulated gate transistors like those envisaged by Tonnel.

Applicants respectfully traverse the Examiner's rejection of Claims 39-41 and 60-62 under 35 U.S.C. § 103. Claims 39-41 and 60-62 depend from Claims 32 and 54 respectively. Since Yamabe et al. provides no teaching with respect to the relative depths of the trench and the body region, for substantially the same reasons discussed above with respect to Claims 32 and 54, Claims 39-41 and 60-62 are each patentable over the combined teachings of Tonnel, Ueda et al., and Yamabe et al.

For the foregoing reasons, Applicants believe that all claims (i.e. Claims 17-42, 44, and 46-65) are allowable and

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respectfully request their reconsideration and allowance. If the Examiner has any questions regarding the above, the Examiner is respectfully requested to telephone the undersigned Attorney at 408-453-9200.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, D.C., 20231, on September 30, 1996.

9/30/96
Date of Signature

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